WHAT IS CLAIMED IS:

1. A probe sheet comprising:

contact terminals that get into contact with electrodes provided on a wafer; wirings drawn from said contact terminals; and electrode pads electrically connected to said wirings,

wherein a pitch of said electrode pads is wider than a pitch of said contact terminals.

2. The probe sheet according to claim 1,

wherein said contact terminals are arranged according to an array of peripheral electrodes of semiconductor devices formed on said wafer and

wherein said electrode pads are arranged in a grid pattern.

3. The probe sheet according to claim 1

wherein a metallic sheet, from which at least a part corresponding to signal electrode pads of the electrode pads is removed, is provided.

4. The probe sheet according to claim 3

wherein a linear expansion coefficient of said metallic sheet is almost equal to a linear expansion coefficient of said wafer.

5. The probe sheet according to claim 3

wherein said metallic sheet is a 42 alloy sheet.

6. The probe sheet according to claim 1

wherein dummy terminals, each of which has a larger contact area with the wafer than said contact

terminal, are provided on a surface on which said contact terminals are provided.

7. The probe sheet according to claim 1

wherein said contact terminals are created each by using an anisotropically etched hole in a crystalline substrate as a cast.

8. A probe card comprising:

a probe sheet having contact terminals that get into contact with electrodes provided on a wafer; and a multi-layer wiring substrate on which electrodes, which are electrically connected to said contact terminals, are provided on a surface opposed to the wafer, and

wherein a pitch of said electrodes provided on the surface of said multi-layer wiring substrate opposed to the wafer is wider than a pitch of said contact terminals.

9. The probe card according to claim 8

wherein said contact terminals are arranged according to an array of peripheral electrodes of semiconductor devices formed on the wafer and

wherein the electrodes of said multi-layer wiring substrate are arranged in a grid pattern.

10. The probe card according to claim 8

wherein the electrodes of said multi-layer wiring substrate are provided in a device-opposed-area on said multi-layer wiring substrate.

11. The probe card according to claim 8,

wherein at least one of capacitors, resistors, or fuses are mounted in the device-opposed area on said multi-layer wiring substrate.

12. The probe card according to claim 8 wherein the electrodes of said contact terminals and the electrodes of said multi-layer wiring substrate are electrically connected by a connection part provided almost vertically with respect said multi-layer wiring substrate.

13. The probe card according to claim 8 wherein a connection between the electrodes of said contact terminals and the electrodes of said multi-layer wiring substrate is made via wires drawn from the contact terminals, electrode pads connected to said wires and having a pitch wider than a pitch of said contact terminals, and spring probes electrically connected to said electrode pads.

14. The probe card according to claim 13 wherein said spring probes are removable.

15. The probe card according to claim 8 wherein a connection between the electrodes of said contact terminals and the electrodes of said multi-layer wiring substrate is made via wirings drawn from said contact terminals, electrode pads connected to said wirings and having a pitch wider than a pitch of said contact terminals, and electrically connected to said electrode pads.

16. The probe card according to claim 8

wherein said probe card has a temperature adjustment function.

17. The probe card according to claim 8

wherein said contact terminals are each a pyramid-shaped or truncated-pyramid-shaped terminal created by using an anisotropically etched hole in a crystalline substrate as a cast.

18. Semiconductor test equipment comprising:

a stage on which a wafer is mounted; and

a probe card having contact terminals that get in contact with electrodes of semiconductor devices formed on the wafer and electrically connected to a tester that tests electrical characteristics of the semiconductor devices

wherein said probe card comprises a probe sheet having the contact terminals; and a multi-layer wiring substrate whose electrodes electrically connected to the contact terminals are provided on a surface opposed to the wafer and

wherein a pitch of the electrodes of said multi-layer wiring substrate provided on the surface opposed to the wafer is wider than a pitch of said contact terminals.

19. Semiconductor test equipment according to claim 18

wherein a temperature of the stage and the probe card can both be controlled.

20. The semiconductor test equipment according to

claim 18

wherein said contact terminals are each a pyramid-shaped or truncated-pyramid-shaped terminal created with an anisotropically etched hole in a crystalline substrate as a shape former.